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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,717	09/25/2003	David A. Luick	ROC920030301US1	6088

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EXAMINER	
ROJAS, MIDYS	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
05/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/670,717	DAVID LUICK	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5 and 7-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5 and 7-9* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/25/03* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The objection to the specification has been withdrawn in view of Applicants amendment to paragraph 0009 of the specification.

Claim Objections

2. The objection to claim 6 has been withdrawn in view of Applicants amendment to the claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 9 recites the limitation "the stream ID indicator" in line 13. There is insufficient antecedent basis for this limitation in the claim.

For examination purposes, the claim will be interpreted as "...checking a valid indicator and if at least one instruction register has the valid indicator set, selecting the thread ID."

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-5, and 7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kissell (US 2007/0043935) in view of Dwyer et al. (6,874,056).

Regarding Claim 3, Kissell discloses a system in a multi-threading execution mode (multiprocessing system with a multithreading processor, Abstract) comprising:

at least one instruction register, the at least one instruction register having a thread ID indicator (ASID, stored in the TASID bits 528 of the TCStatus Register 508, paragraph 0058);

an address generator (CPU generates virtual address) having a cache index indicator (data portion) and a plurality of cache index bits (tag portion, paragraph 0141);

a cache memory (TLB 1202);

and a selector for selecting between the thread ID indicator and the cache index indicator, the selector outputting an upper index indicator, wherein when the thread ID indicator is selected by the selector (the ASID is selected based on the current processor thread, paragraph 0140), the thread ID indicator is output to the upper index indicator, and the upper index indicator is concatenated with the plurality of cache index bits to form an address for retrieving an entry from the cache memory (tag portion including virtual page address or virtual page number is concatenated with ASID... virtual memory address to make an access, the virtual memory address is concatenated with the ASID of the process making the memory access, and the result is compared with the TLB to see if a match occurs, paragraph 0141).

Kissell does not teach a cache miss counter wherein the cache miss counter controls the selector.

Dwyer et al. discloses a cache thrashing reductions system in which cache miss counters are kept (Col. 4, lines 59-65 and Col. 5, lines 45-56) to aid in the selection of sets for the

reductions of thrashing (selecting sets based on access rates, Col. 2, lines 25-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow for the selector to take into account cache misses in its selection since doing so allows the system to assume that high miss rates represent sets that are experiencing thrashing and therefore need thrash reduction (Col. 2, lines 14-16).

Regarding Claim 2, Kissell discloses the apparatus further comprising a machine state register (cpus_allowed mask), the machine state register having an enable indicator that controls the selection of the ASID. In clearing the cpus_allowed mask, the operating system is enabled to select the ASID depending on the thread (paragraph 0162).

Regarding Claim 4, Kissell discloses the apparatus wherein each thread ID indicator (ASID) further comprises a plurality of bits (ASID stored in the TASID **bits** 528 of the Tcstatus register 508, Figure 5J).

Regarding Claim 5, Kissell discloses the apparatus wherein each thread ID indicator (ASID) further comprises a single bit (ASID stored in the TASID **bits** 528 of the Tcstatus register 508 wherein bits comprise a number of single bits, Figure 5J).

Regarding Claim 7, Kissell discloses a system in a multi-threading execution mode (multiprocessing system with a multithreading processor, Abstract) comprising:

at least one instruction register, the at least one instruction register having a thread ID indicator (ASID, stored in the TASID bits 528 of the TCStatus Register 508, paragraph 0058);

an address generator (CPU generates virtual address) having a cache index indicator (data portion) and a plurality of cache index bits (tag portion, paragraph 0141);

a cache memory (TLB 1202);

and a selector for selecting between the thread ID indicator and the cache index indicator, the selector outputting an upper index indicator, wherein when the thread ID indicator is selected by the selector (the ASID is selected based on the current processor thread, paragraph 0140), the thread ID indicator is output to the upper index indicator, and the upper index indicator is concatenated with the plurality of cache index bits to form an address for retrieving an entry from the cache memory (tag portion including virtual page address or virtual page number is concatenated with ASID... virtual memory address to make an access, the virtual memory address is concatenated with the ASID of the process making the memory access, and the result is compared with the TLB to see if a match occurs, paragraph 0141).

Kissell does not teach an enable cache indicator that controls the selection of the selector.

Dwyer et al. discloses using a valid bit 340 (enable indicator) for invalidating sets from being selected (Col. 4, lines 45-56 and Col. 5, lines 5-13). In invalidating the sets from selection, the valid bit is controlling the selector since the invalidated sets cannot be selected. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the invention of Kissell to include the valid bit of Dwyer since doing so prevents the selection of invalid sets.

Regarding Claim 8, Kissell does not teach a cache miss counter wherein the cache miss counter controls the selector. Dwyer et al. discloses a cache thrashing reductions system in which cache miss counters are kept (Col. 4, lines 59-65 and Col. 5, lines 45-56) to aid in the selection of sets for the reductions of thrashing (selecting sets based on access rates, Col. 2, lines 25-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow for the selector to take into account cache misses in its selection since doing

so allows the system to assume that high miss rates represent sets that are experiencing thrashing and therefore need thrash reduction (Col. 2, lines 14-16).

Claim 10 is rejected using the same rationale as that of Claim 7.

Allowable Subject Matter

7. The indicated allowability of claims 3, and 7-9, of which limitations were incorporated into newly amended independent claims 3, 7, and 9, is withdrawn in view of the newly discovered reference(s) to Dwyer et al. (6,874,056). Rejections based on the newly cited reference(s) are presented above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Midys Rojas
Examiner
Art Unit 2185

MR

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